1. A computer memory chip comprising

(i) a plurality of memory cells in a predetermined arrangement,

(ii) a plurality of programmable connection devices at selected locations in the memory chip, and

(iii) programmable control logic to enable the memory cells to be addressed and interfaced to a data processing device,

whereby the width of the memory chip may be reconfigured.

2. A computer memory chip as set forth in claim 1, wherein said programmable connection devices comprise PASS transistors.

3. A computer memory chip as set forth in claim 1, wherein said programmable connection devices comprise multiplexers.

4. A method for configuring a computer memory chip, comprising the steps of

(a) providing a computer memory chip with

(i) a plurality of memory cells in a predetermined arrangement

(ii) a plurality of programmable connection devices at selected locations in the memory chip, and

(iii) programmable control logic to enable the memory cells to be addressed and interfaced to a data processing device, and

(b) programming selected programmable connection devices to reconfigure the arrangement of the memory cells to a selected configuration, and to configure the control logic to interface the memory cells in that selected configuration to a data processing device in a predetermined manner.

5. A method as set forth in claim 4, wherein the step of programming selected memory devices is adapted to reconfigure the width of the memory chip.

6. A field programmable memory cell array, comprising in combination:

a plurality of memory cells in a predetermined arrangement including input and output;

a programmable address decoder for enabling addressing of said memory cells; and

a programmable I/O controller for interfacing said input and output of said plurality of memory cells.

7. The array as set forth in Claim 6, wherein said programmable address decoder comprises multiplexers and decoders for addressing said memory cells and wherein said programmable I/O controller comprises switch means for reconfiguring said input and output.

8. A method for configuring the array of Claim 6, comprising the steps of programming said programmable address decoder and said programmable I/O controller to reconfigure said arrangement of memory cells to a selected configuration and to configure said control logic to interface said memory cells in said selected configuration.

9. The array as set forth in Claim 6, wherein said array is configured as a variable-width memory device.

10. The array as set forth in Claim 6, wherein said array is configured as a dynamically configurable cache device.

11. The array as set forth in Claim 6, wherein said array is configured as a reconfigurable memory device.

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